(U.S. Patent No. 5,959,329). Claims 1 – 5 and 7 – 19 remain pending, with claims 8 – 19 withdrawn from consideration as directed to a non-elected invention.

Regarding the claims, Applicants respectfully traverse the rejection of claims 1 – 7, as detailed above, for the following reasons.

Regarding the 35 U.S.C. § 103(a) rejection of claims 1 – 5 and 7, Applicants respectfully disagree with the Examiner's arguments and conclusions. A *prima facie* case of obviousness has not been made, since the Examiner does not show that all the elements of Applicants' claims are met in the cited reference, and does not show that there is any suggestion or motivation to modify the cited reference to result in the claimed invention. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. ... If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious." See M.P.E.P. § 2143.03, 8th Ed., Aug. 2001, p. 2100-26.

Applicants' claim 1 recites a combination of elements, including, *inter alia*, "a semiconductor substrate having a main plane in which a channel of a transistor is formed, the semiconductor substrate comprising a first region and a second region defined in a section taken along a direction of a channel length, the second region having a surface located lower than that of the first region, and the second region being connected to the first region."

For the purposes of clarification, Applicants refer the Examiner to the attached Reference Figures 1 and 2, which are plan views of the present invention and the invention disclosed in Rhee, respectively. Figure 2A of the present invention is a cross-sectional view illustrating an exemplary embodiment of the invention according to claim 1; and the cross section shown in Applicants' Figure 2A corresponds to the A-A' section line drawn in Reference Figure 1. The cross section of Rhee's invention, e.g. Rhee's Figure 7, corresponds to the B-B' section shown in

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Reference Figure 2. It is apparent from the reference figures that the cross section shown in Figure 2A of Applicants' invention is taken in the *direction of channel length*, whereas the cross section shown in Rhee's Figure 7 is taken in the direction *perpendicular* to the direction of the channel length. The angle at which the present invention is viewed, as shown, for example, in Figure 2A, differs from the angle at which Rhee's invention in Figure 7 is viewed. Therefore, Applicants' Figure 2A and Rhee's Figure 7 cannot be compared to illustrate the recitations of Applicants' claimed invention.

Applicants refer the Examiner to Rhee's Figure 7, specifically the central region around gate electrodes 62 and 64, which is a cross-sectional view of high breakdown voltage MOS transistors (Rhee, column 7, lines 7 – 8). This cross-section is taken in the direction of the channel width. A p-type semiconductor substrate 40 and P-well 42 are shown with a flat area between low-concentration impurity layers 55 on the left and right. Rhee does not disclose anything about the structure, layout, or regions of semiconductor substrate 40, P-well 42, gate insulating film 60, or poly-Si gate electrodes 62 and 64, in a section taken along a direction of a channel length (when viewing Rhee's Figure 7, the channel length cross-sectional view would be in the direction perpendicular to the paper). As such, Rhee does not disclose a first or second region on semiconductor substrate 40 or P-well 42 "defined in a section taken along a direction of a channel length, the second region having a surface located lower than that of the first region, and the second region being connected to the first region," which is recited, *inter alia*, in Applicants' claim 1. One can only discern one region on P-well 42 taken in the direction of the channel *width*, and not any information in the direction of the channel *length*.

In contrast, Applicants refer the Examiner to Figure 2A showing an exemplary embodiment of the present invention, which depicts a cross-sectional view taken along the

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

channel *length*. Substrate 1 is clearly shown with two regions, the second region having a surface located lower than that of the first region, and the second region being connected to the first region.

Furthermore, Rhee does not teach or suggest "a post oxide film formed on the second region, containing silicon and oxygen and arranged to be in contact with the gate electrode and the gate insulating film," as recited, *inter alia*, in Applicants' claim 1. According to Rhee's Figure 7, there is no post oxide film either covering (along channel length cross-sectional view, if it were shown) or deposited next to (along the channel width cross-sectional view, as shown) poly-Si gate electrodes 62 and 64.

Teramoto fails to cure the deficiencies of Rhee, since Teramoto also does not teach or suggest the recitations of Applicants' present invention which are not taught or suggested in Rhee. Furthermore, even though Teramoto does not disclose or suggest all the features of Applicants' claimed invention, the inclusion of Teramoto does not render the recitations of Applicants' independent or dependent claims obvious when combined with Rhee. Merely because Teramoto discloses a "thin gate insulating film 506 of SiO_xN_y" (Teramoto's Figure 10C and column 18, line 37), does not mean that one would find it obvious to then use Teramoto's film in combination with Rhee to result in Applicants' claimed invention. Thus, Rhee and Teramoto, taken alone or in combination, do not teach or suggest at least these elements of Applicants' claim 1. The Examiner's application of Rhee and Teramoto as references in a 35 U.S.C. § 103(a) rejection is improper.

The Examiner has therefore not met at least one of the essential criteria for establishing a *prima facie* case of obviousness, wherein "the prior art reference (or references when combined) must teach or suggest all the claim limitations." See M.P.E.P. §§ 2142, 2143, and 2143.03.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Furthermore, there is no suggestion or motivation to modify Rhee to produce Applicants' claimed invention. Even if the Examiner's characterization of Rhee (see Final Office Action, item 2, p. 3) were correct (which Applicants dispute), this still does not establish that there would have been the requisite suggestion or motivation to modify Rhee with Teramoto. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." M.P.E.P. § 2143.01, p. 2100-124, citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Even modifying Rhee to "include silicon, nitrogen, and oxygen" (Office Action, item 2, p. 4), as the Examiner suggests, would still not produce Applicants' present invention.

Teramoto's disclosure is clearly different from Applicants' claimed invention, as it does not suggest the desirability of any modification to result in Applicants' present invention. In addition, Teramoto actually teaches away from the present invention. Teramoto discloses that "it is recommended to oxidize the surface of the active semiconductor layer by irradiating it [with] lasers or ... intense rays comparable to lasers in an oxidizing ... atmosphere ... before forming the gates insulating film thereon" (Teramoto, col. 5, ll. 7 – 12). Furthermore, Teramoto discloses "[t]he silicon oxide film thus formed ... is almost comparable to a silicon oxide film to be obtained by thermal oxidation" (Teramato, col. 5, ll. 37 – 42). In support of this, Teramoto teaches that "[t]o form this oxide film, both sputtering ... and depositing ... by plasma CVD ... followed by annealing the deposited film at 450°C to 650°C are employable" (Teramoto, col. 6, ll. 37 – 41). In contrast, Applicants' specification notes the problems with conventional oxidation methods, e.g. thermal oxidation, such as those taught by Teramoto. See, for example, Applicants' specification on p. 2, l. 9 to p. 4, l. 27. Thus, Teramoto does not provide the requisite motivation for its modification. Furthermore, the teaching away noted above

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

demonstrates that there is not any reasonable expectation of success from so doing to produce Applicants' claimed invention.

Furthermore, the M.P.E.P. states "[a] statement [by the Examiner] that modifications of the prior art to meet the claimed invention would have been "'well within the ordinary skill of the art at the time the invention was made'" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references." M.P.E.P. § 2143.01, p. 2100-124 (citations omitted, emphasis in original). Because Applicants have already established that Rhee or Teramoto cannot be modified to produce the present invention, Applicants submit that, according to the M.P.E.P., the Examiner's reliance on Rhee and Teramoto fails to establish *prima facie* obviousness.

Applicants have demonstrated herein that the Examiner: (a) has not shown all recitations of Applicants' claimed invention are taught or suggested by Rhee and Teramoto, taken alone or in combination; (b) has not shown any requisite motivation to modify Rhee with Teramoto; and (c) has not shown there would be any reasonable expectation of success from modifying Rhee with Teramoto, in order to produce Applicants' claimed invention.

Furthermore, regarding the rejection of dependent claims 2 – 5 and 7, "Examiners are reminded that a dependent claim is directed to a combination including everything recited in the base claim and what is recited in the dependent claim. It is this combination that must be compared with the prior art, exactly as if it were presented as one independent claim." M.P.E.P. § 608.01(n)(III), p. 600-77. Applicants have already demonstrated that Rhee and Teramoto, taken alone or in combination, cannot produce Applicants' present invention. Therefore, the

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

addition of Takemura and Tomita in the rejections of dependent claims 5 and 7, respectively, still does not render Applicants' claimed invention obvious.

At least for the abovementioned reasons, Applicants respectfully submit that independent claim 1 should be allowed, as should claims 2 – 5 and 7, at least by virtue of their dependence from allowable base claim 1.

In view of the foregoing, Applicants submit that the rejection of claims 1 – 5 and 7 is improper and should be withdrawn. Applicants submit that independent claim 1 is in condition for allowance as are claims 2 – 5 and 7, at least by virtue of their dependence from allowable base claim 1.

Applicants respectfully request that this Request for Reconsideration after Final be entered by the Examiner, placing claims 1 – 5 and 7 in condition for allowance. This Request for Reconsideration after Final should allow for immediate and favorable action by the Examiner. Applicants submit that the entry of this Request would place the application in better form for appeal, should the Examiner continue to dispute the patentability of the pending claims. Applicants, therefore, request the entry of this Request, the Examiner's reconsideration of the application, and the timely allowance of the pending claims.

Please grant any extensions of time under 37 C.F.R. § 1.136 required in entering this response. If there are any fees due under 37 C.F.R. § 1.16 or 1.17, which are not enclosed

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

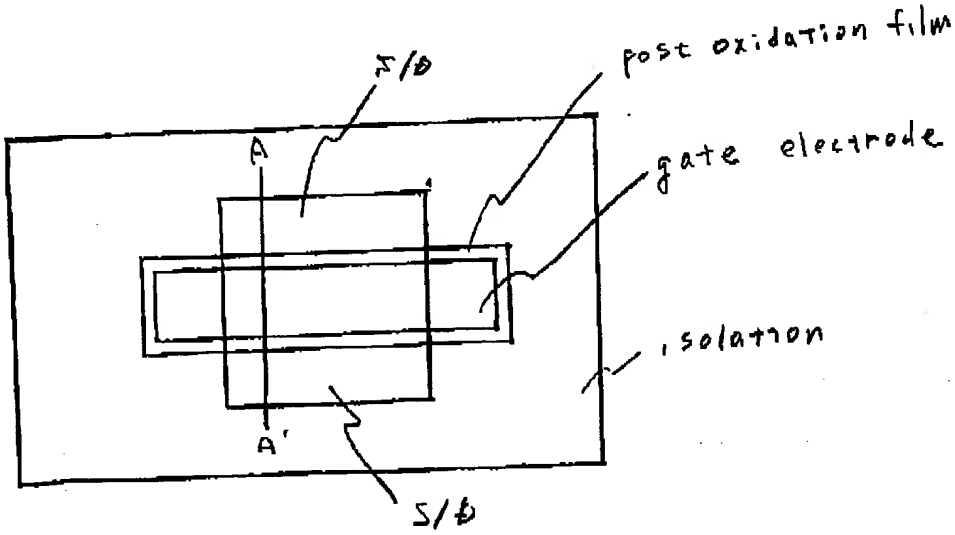
Dated: March 28, 2002

By: Robert J. Rotella Reg # 24,014
for Richard V. Burgujian
Reg. No. 31,744

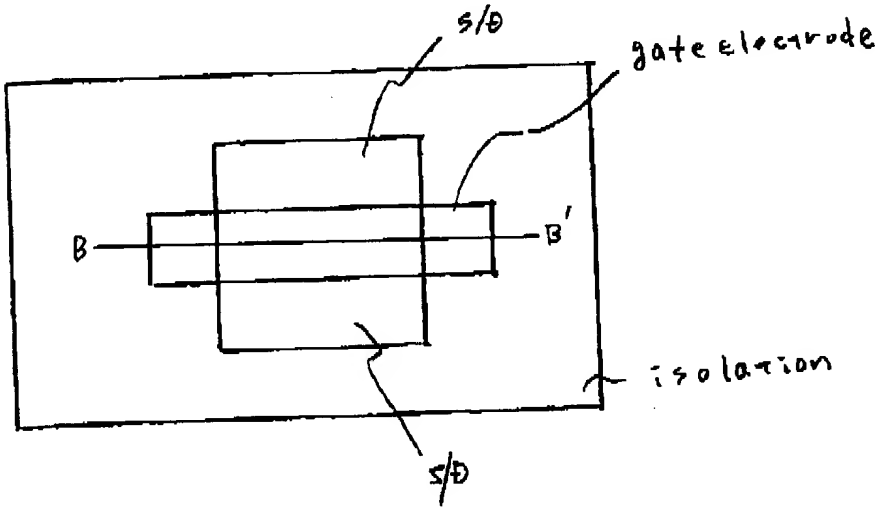
FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

reference figure 1 (present invention)



reference figure 2 (prior art)



** TOTAL PAGE.06 **